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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/525,802	03/15/2000	Itsuo Hidaka	AKM-00301	9924

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EXAMINER
CRUZ, LOURDES C

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 07/02/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/525,802	HIDAKA, ITSUO
	Examiner	Art Unit
	Lourdes C. Cruz	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-9 and 13-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16* is/are allowed.

6)☒ Claim(s) *1,2,5-9 and 13-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the plurality of transistors, and passive semiconductor devices disposed upon a substrate of claims 5,8,10 and 18 must be shown or the features canceled from the claims. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 5-15 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. See that the specification does not provide support for

the plurality of transistors, and passive semiconductor devices disposed upon a substrate in a way that one with skill in the art would be able to make the invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 recites "the edge". This term lacks antecedent basis.

Regarding claim 13, "the second" and "the fourth" lack antecedent basis in the claim.

Also, see that some of the claims now depend upon cancelled claims. This makes the claims indefinite for depending upon now inexistent limitations.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Cronin et al. (US 4776087).

Cronin discloses a semiconductor device having multiple wiring layers, comprising: a signal line 56A which is formed in a wiring layer and to which a signal voltage is applied; two adjacent lines 56 which are so adjacent to said signal line as not to be connected thereto, and which are formed in the wiring layer where said signal line is formed –See Fig. 6--; two intersection lines 52 which are respectively formed in wiring lines, each being present via an insulating layer 54 above or under the wiring layer where said signal line and said adjacent lines are formed, and which are formed along a surface area corresponding to an area which is enclosed by said two adjacent lines; and a plurality of entire-line-area through holes penetrating through insulating layer 54,58 formed between said adjacent and intersection lines, and which respectively and electrically connect said adjacent and said intersection lines, wherein said signal line is completely enclosed by said two adjacent lines, said two intersection lines and said through holes, which are one of conductors and semiconductors.

Regarding claim 2, see Fig. 6 wherein the prior art shows said two adjacent lines disposed substantially in parallel to said signal line.

See that Cronin et al. discloses all the structural limitations of claim 1. Claim 1, however, recites an intended use limitation. See that such limitation has no patentable weight and does not distinguish what is claimed from that disclosed by the prior art.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-9, 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cronin et al. in view of Ma (US 5729047).

Cronin et al. discloses:

A semiconductor device having multiple wiring layers, comprising: a signal line 56A which is formed in a wiring layer and to which a signal voltage is applied; two adjacent lines 56 which are so adjacent to said signal line as not to be connected thereto, and which are formed in the wiring layer where said signal line is formed –See Fig. 6--; two intersection lines 52 which are respectively formed in wiring lines, each being present via an insulating layer 54 above or under the wiring layer where said signal line and said adjacent lines are formed, and which are formed along a surface area corresponding to an area which is enclosed by said two adjacent lines; and a plurality of entire-line-area through holes penetrating through insulating layer 54,58 formed between said adjacent and intersection lines, and which respectively and electrically connect said adjacent and said intersection lines, wherein said signal line is completely enclosed by said two adjacent lines, said two intersection lines and said through holes, which are one of conductors and semiconductors. See Fig. 6 wherein the

prior art shows said two adjacent lines disposed substantially in parallel to said signal line.

Cronin et al. also discloses transistors and passive semiconductor devices disposed upon a substrate – See Col. 4, lines 5+--.

However, Cronin describes a single shielded conductor. Ma discloses many such shielding structures for the purpose of decoupling conductors from one another – See Fig. 16-- It would have been obvious to one with ordinary skill in the art to expand Cronin's layering technique to shield multiple conductors from one another as shown by Ma.

Further regarding claims 5,7,15 and 18 the claims recite an intended use limitation. See that such limitation has no patentable weight and does not distinguish what is claimed from the prior art. Additionally, see that it would be obvious to that conductors within the same shield would be in the same phase, since conductors having signals of the same phase need not be shielded from one another but need to be shielded from external influence.

Regarding claim 8, " the phrase signal voltage having different..." encompasses an intended use limitation; as for such has no patentable weight. Additionally, it would be obvious to shield the conductors, as claimed in claim 8, from one another since conductors of different phase not shielded from each other would cause interference.

Regarding claims 6 and 9 the shields of both Cronin and Ma are retained at a predetermined potential independent from the potential applied to the signal line.

Regarding claim 14, it would be obvious to one with ordinary skill in the art that the signals could be either in or out of phase.

Claim 16 **is allowed.**

Response to Arguments

Applicant's arguments filed 4-8-02 have been fully considered but they are not persuasive. Applicant traverses the objection to the drawings on the grounds that drawings may be required when helpful in understanding the invention. Applicant is referred to 37 CFR 1.83(a), wherein it is stated clearly that the drawings must show every feature of the invention specified in the claims.

Applicant also traverses the rejection under 112, first paragraph on the grounds that one of ordinary skill in the art will have no trouble understanding includes and is built above and using standard semiconductor technology. This is not persuasive because, as explained above, the specification must provide support for the plurality of transistors, and passive semiconductor devices disposed upon a substrate.

Applicant argues that Cronin fails to teach electric potential values with potential sources having a selected potential value and the electric potential having a same phase of the potential of the signal line. See that any potential value is a selected potential value. This includes no potential value as well. Also, reciting the intended

electric potential phase at which the signal line, or any other structure, is to be kept, does not distinguish the present invention from the prior art because such recitation only recites intended use limitations which do not structurally differentiate the invention from the prior art (see rejection above).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lourdes C. Cruz whose telephone number is 703-306-5691. The examiner can normally be reached on M-F 8:00- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers

for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Lourdes Cruz
July 1, 2002

Lourdes C. Cruz
Examiner
Art Unit 2827

Albert W. Paladini 7-1-02

ALBERT W. PALADINI
PRIMARY EXAMINER